AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method of forming a ~~process~~ wafer for integrated circuits comprising low voltage elements and high voltage elements, wherein chip regions ~~(6, 7)~~ of different ~~potential~~ potentials are separated by dielectrically insulating regions [[(T) by]] formed as isolation trenches extending downward from a first planar surface [[(F)]], at least one of said isolation trenches ~~having or~~ receiving a material that is ~~oxidzable~~ oxidizable in an oxygen containing atmosphere at an elevated temperature, said method comprising a sequence of ~~main~~ process steps after forming at least two vertical insulating layers in said at least one of said isolation trenches ~~(4a, 4b)~~ and a horizontal insulating layer on said first planar surface to provide a second planar surface of an insulating layer above said first planar surface, ~~(4a', 4b')~~ said sequence comprising:

[[-]] filling said at least one isolation trench with a fill material [[(5)]] until a deepest point of an indentation ~~(5c) of a~~ in a resulting fill material layer ~~(5', 5")~~ formed on [[the]] said first planar surface ~~is positioned with its top side~~ has a first level that is above a second level defined by ~~the~~ said second planar surface ~~formed by the insulating layers (4)~~;

[[-]] performing a first planarization ~~process on the~~ of said resulting fill material layer [[(5)]];

[[-]] removing a first portion of [[the]] fill material [[–]] ~~as a vertical fill layer (5*)~~ [[–]] in said at least one of said isolation trenches by a first over-removal ~~process~~ down to a defined depth [[(h7)]];

[[-]] removing a portion of at least the vertical insulating layers ~~(4a, 4b, 4a', 4b')~~ and ~~further~~ over-removing [[of]] a further portion of the fill material ~~layer (5*)~~ so as to ~~obtain or~~ reach a ~~substantially equal~~ height level ~~(h10) of the~~ substantially equal with said vertical insulating layers ~~(4; 4a, 4b; 5)~~ within said at least one of said isolation trenches;

[[-]] depositing at least one [[a]] cap layer ~~or a layer system as a cover~~ having a thickness extending above ~~the level of the~~ said first planar surface [[(F)]] and extending

downward[[ly]] to ~~the substantially equal height level~~ said vertical insulating layers and said fill material within [[the]] said at least one of said isolation trenches; and

[[-]] performing a further planarization ~~process on the cover~~ of said cap layer [[(9)]] by one of a chemical mechanical polishing process [[or]] and a resist planarization process to form a cover.

2. (Currently Amended) The method of claim 1, wherein said cover [[(9)]] is an oxygen impermeable cap in the form of a layer system~~, in particular in the form of a plurality of stacked layers~~.

3. (Currently Amended) The method of claim 1, wherein said cover is an oxygen impermeable cap ~~cover (9) is~~ provided as a layer comprised of silicon nitride.

4. (Currently Amended) The method of ~~claims 1 or 2~~ claim 1, wherein said cover [[(9)]] is oxygen impermeable and ~~said oxygen impermeable layer~~ comprises a plurality of layers at least one of said plurality of layers having a different specific characteristic than at least one other layer~~, such as a specified coefficient of extension or getter capabilities for ions~~.

5. (Currently Amended) The method of claim 1, wherein said process wafer is ~~an~~ a silicon on insulator [[SOI]] wafer including a buried insulating layer [[(2)]] formed on a carrier layer [[(1)]].

6. (Currently Amended) The method of claim 1, wherein the fill material ~~(4, 5*) of said at least one isolation trench (5a) having said cover (9)~~ in said trench and said cover is adjusted so as to reduce ~~and preferably minimize~~ a bending of the ~~semiconductor~~ wafer during further processing.

7. (Currently Amended) The method of claim 1, wherein [[the]] surfaces of [[the]] said cover [[(9)]] and [[the]] exposed chip regions ~~(6, 7)~~ define a continuous plane [[(F)]] for low voltage elements and high voltage elements~~, said plane preferably lacking a step in the trench area and adjacent thereto~~.

8. (Currently Amended) The method of claim 1, wherein said vertical and horizontal insulating layers ~~(4; 4a, 4b, 4a', 4b')~~ are formed by a thermal oxidation.

9. (Currently Amended) The method of claim 1, wherein said fill material ~~(5; 5', 5'', 5*)~~ is polysilicon.

10. (Currently Amended) The method of claim 1[[m]], wherein ~~the concurrent~~ removal of [[the]] said vertical insulating layers ~~(4a, 4b, 4a', 4b')~~ and ~~the vertical~~ fill material in said at least one of said isolation trenches ~~layer (5*)~~ is performed with a defined measure of depth removal by an etch process~~, preferably across the entire trench width~~.

11. (Currently Amended) The method of claim 1, wherein ~~only a~~ no more than one mask is used for forming said at least one of said isolation trenches ~~(5a) is used for the process steps of claim 1~~.

12. (Currently Amended) The method of claim 1, wherein ~~the first and the second~~ removal of [[the]] said fill material [[(5*)]] located within [[the]] said at least one of said isolation trenches ~~are defined etch back processes~~ is a defined etching back.

13. (Currently Amended) The method of claim 1, wherein said cover ~~(9) lowered into~~ positioned within said trench performs [[a]] both vertically ~~or~~ and laterally acting insulation across an entire trench width [[(9b)]].

14. (Currently Amended) The method of claim 1, wherein said cover [[(9)]] is dielectrically insulating.

15. (Original) The method of claim 1, wherein said low voltage elements are logic elements.

16. (Currently Amended) The method of claim[[s]] 1[[or 15]], wherein said high voltage elements are power elements.

17. (Currently Amended) The method of claim 1, wherein [[the]] said low voltage elements and said high voltage elements are located ~~or are formed~~ in an active semiconductor layer[[(3)]].

18. (Currently Amended) The method of ~~claims 1 or~~ claim 17, wherein said active semiconductor layer [[(3)]] extends horizontally and is bordered in [[the]] a vertical direction by a buried insulating layer[[(2)]].

19. (Currently Amended) The method of claim 1, wherein at least one of said isolation trenches ~~(T, 5a)~~ is formed in an active semiconductor layer [[(3)]] to a lower end thereof at a buried insulating layer [[(2)]].

20. (Currently Amended) The method of claim 1, wherein said fill material [[(5*)]] is one of electrically conductive~~, in particular is a polysilicon, or is (slightly)~~ and oxidizable.

21. (Currently Amended) The method of ~~claims~~ claim 1, wherein ~~during the first removal (over-removal) of the~~ removal of said first portion of fill material within said at least one of said isolation trenches ~~(5a) the removal isperformed~~ is not deeper [[(h7)]] than down to half of [[the]] a trench depth~~, in particular to approximately ¼ of the trench depth or less~~.

22. (Currently Amended) The method of ~~claims 1 or 21~~ claim 1, wherein ~~during the further removal (over-removal) material~~ over-removal of said further portion of said fill material within said at least one of said isolation trenches reaches ~~is removed~~ not deeper [[(h9)]] than down to half of the trench depth~~, in particular to approximately ¼ of the trench depth or less~~.

23. (Currently Amended) The method of claim 1, wherein ~~said~~ a trench depth [[(h0)]] in ~~the~~ an active semiconductor layer [[(3)]] is greater than [[1]] 10 µm~~, in particular greater than 10µm or is substantially 50µm~~.

24. (Currently Amended) The method of ~~claims 1 or 23~~ claim 1, wherein said at least one isolation trench [[(5a)]] has an aspect ratio of depth to width that is ~~higher~~ greater than 10:1. ~~10:1, and in particular higher than 15:1.~~

25. (Currently Amended) The method of ~~claims 1 or 19~~ claim 1, wherein said vertical insulating layers ~~(4a, 4b)~~ at both trench walls are ~~or have been~~ formed down to [[the]] a horizontal insulating layer ~~(2), when said main process steps start~~.

26. (Currently Amended) A ~~process~~ wafer ~~(1, 2, 3)formed or formable according to any of the preceding method claims~~ for integrated circuits comprising low voltage elements and high voltage elements, wherein chip regions of different potentials are separated by dielectrically insulating regions formed as isolation trenches extending downward from a first planar surface, at least one of said isolation trenches receiving a material that is oxidizable in an oxygen containing atmosphere at an elevated temperature and two vertical insulating layers formed in said at least one of said isolation trenches and a horizontal insulating layer on said first planar surface to provide a second planar surface of an insulating layer above said first planar surface prepared by a process comprising the steps of:

filling said at least one isolation trench with a fill material until a deepest point of an indentation in a resulting fill material layer formed on said first planar surface has a first level that is above a second level defined by said second planar surface;

performing a first planarization of said resulting fill material layer;

removing a first portion of fill material in said at least one of said isolation trenches by a first over-removal down to a defined depth;

removing a portion of at least the vertical insulating layers and over-removing a further portion of the fill material so as to reach a height level substantially equal with said vertical insulating layers within said at least one of said isolation trenches;

depositing at least one cap layer having a thickness extending above said first planar surface and extending downward to said vertical insulating layers and said fill material within said at least one of said isolation trenches; and

performing a further planarization of said cap layer by one of a chemical mechanical polishing process and a resist planarization process to form a cover.

27. (Currently Amended) A method for treating [[an]] a silicon on insulator ~~SOI~~ wafer ~~(1, 2, 3)~~ and forming therein dielectrically insulating isolation trenches ~~(5a, T)~~ between two regions ~~(6, 7)~~ of [[the]] an active semiconductor layer of the ~~SOI~~ wafer, said regions being associated with ~~respective~~ two different potentials ~~(P1, P2)~~, respectively, said method comprising:

forming vertical insulating layers ~~(4a, 4b)~~ laterally on walls of at least one of said isolation ~~formed~~ trenches; ~~structure (5a),~~

filling ~~a gap in the~~ said at least one of said isolation trenches with a fill layer between said vertical insulating layers; [[(5*),]]

removing the fill layer [[(5*)]] down to a certain trench depth ~~(h9, h7)~~ together with a portion of the vertical insulating layers on the lateral walls of said at least one of said isolation trenches ~~wall insulation (4a, 4b)~~ so as to obtain a substantially equal height level [[(h10)]] of the upper ends of ~~the three layers being present in said trench~~ said fill layer and said vertical insulating layers;[[, and]]

depositing a cap layer [[(9)]] on said active semiconductor layer at least over and in the vicinity of said ~~on the~~ upper ends of said fill layer and said vertical insulating layers ~~and in the vicinity of the active semiconductor layer (3);~~ and

~~including a removal (planarization) of~~ removing said cap layer down to a laterally extending planar surface ~~(F) above the filled trench and at least within [[the]] a neighbouring area at both trench sides so as~~ to expose said active semiconductor layer [[(3)]] adjacent to ~~the respective insulation~~ said at least one isolation trench.

28. (Currently Amended) An at least partially processed silicon on insulator ~~SOI~~ wafer for further processing comprising a trench structure [[(T)]] including within ~~the~~ said trench structure an insulating layer sequence of vertically oriented first layers ~~(%+, 4a, 4b)~~ that are covered at [[the]] a top side thereof by a second layer [[(9)]] laterally extending to ~~and on~~ the walls of ~~the~~ said trench structure, thereby forming a planar surface [[(F)]] of the ~~SOI~~ wafer, two of said first layers ~~(4a, 4b)~~ extending down to a buried insulating layer [[(2)]] of the ~~SOI~~ wafer.

29. (Currently Amended) The method of claim[[s]] 1[[or 11]], wherein depositing at least one of a cap layer and a layer system as a [[said]] cover [[(9)]] is performed without a mask.

30. (Cancelled)

31. (Currently Amended) A method of forming electric circuits, said electric circuits having integrated therein low voltage logic elements and high voltage power elements~~, the~~ and having chip regions of different ~~potential~~ potentials being separated from one another by dielectrically insulating ~~regions by~~ isolation trenches extending from [[the]] a planar surface and including materials capable of oxidizing at elevated temperatures in an oxygen containing atmosphere, said method ~~being characterized by a sequence of the following main processes after~~ including forming ~~the~~ insulating layers [[(4)]] and further comprising:

[[-]] filling said isolation trenches with [[a]] fill material [[(5)]] until [[the]] a deepest portion of indentations of [[the]] formed fill material layers [[is]] are positioned ~~at its top side~~ above ~~the level of the~~ a planar surface defined by ~~the oxide layer (4)~~ said insulating layers;

[[-]] planarizing the fill material [[(5)]];

[[-]] removing said fill material in [[the]] said isolation trenches to a defined depth by over-etching;

[[-]] etching said ~~oxide~~ insulating layers [[(4)]] and over-etching said fill material [[(5)]] so as to obtain a substantially equal height level of [[the]] said insulating layers [[(4)]] and said fill material [[(5)]] within [[the]] said isolation trenches;

[[-]] depositing [[the]] at least one of a cap layer ~~(9) or~~ and a layer system with a thickness that extends above the level of [[the]] said planar surface; and

[[-]] planarizing said at least one of the cap layer [[or]] and the layer system by at least one of a chemical mechanical polishing ~~or by performing~~ and a resist planarization process.

32. (Currently Amended) The method of claim 31, ~~characterized in that the oxygen impermeable cap layer is a layer system, i.e., is comprised of~~ wherein said at least one of the cap layer and the layer system comprises a plurality of stacked layers~~, wherein said~~ including an oxygen

impermeable layer ~~is combined with~~ and layers of other specific characteristics~~, such as specific coefficients of expansion and getter capabilities for ions~~.

33. (Currently Amended) The method of claim 31, ~~characterized in that~~ wherein said at least one of the cap layer and the layer system is [[the]] an oxygen impermeable [[cap]] layer ~~is layer~~ comprised of silicon nitride.

34. (New) The method of claims 2, wherein the layer system has a plurality of stacked layers.

35. (New) The method of claim 4, wherein said different specific characteristic comprises a specified coefficient of extension.

36. (New) The method of claim 4, wherein said different specific characteristic comprises getter capabilities for ions.

37. (New) The method of claim 7, wherein the continuous plane lacks steps in a trench area and adjacent areas.